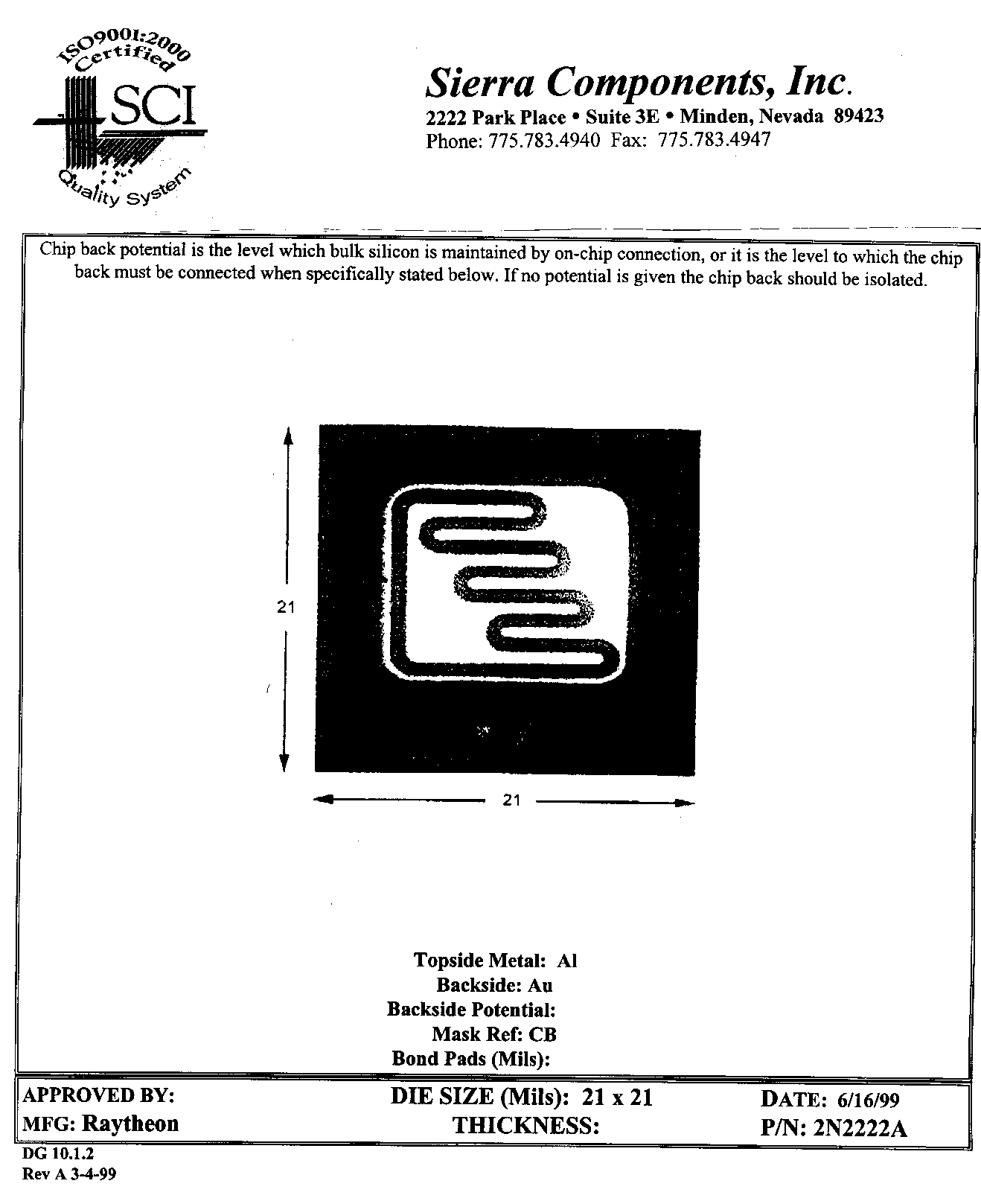
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.021”**



**.021”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .004 X .004”**

**Backside Potential:**

**Mask Ref: CB**

**APPROVED BY: DK DIE SIZE .021” X .021” DATE: 1/26/22**

**MFG: RAYTHEON THICKNESS .008” P/N: 2N2222A**

**DG 10.1.2**

#### Rev B, 7/1